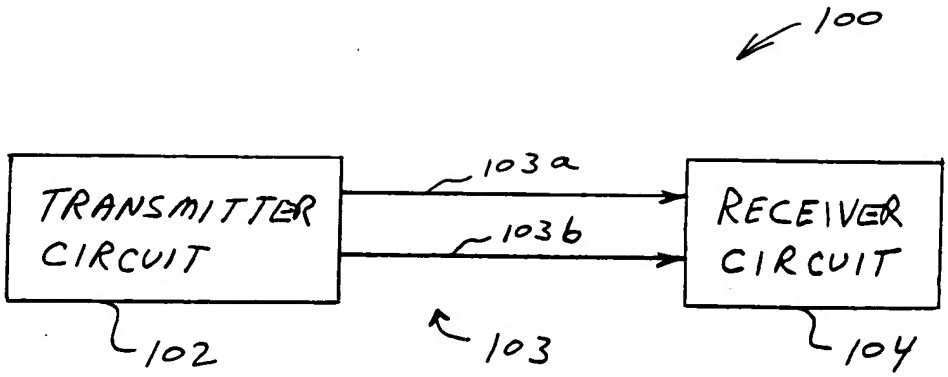
100
TRANSMITTER CIRCUIT
103a
103b
RECEIVER CIRCUIT
102
103
104

FIG. 1

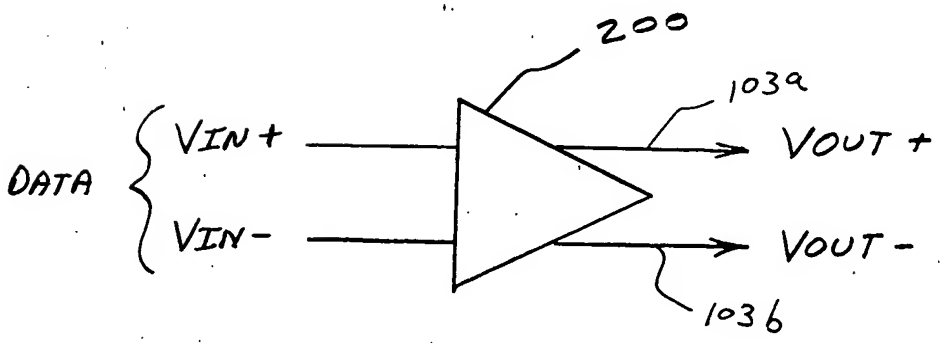
200
103a
DATA
VIN+
VIN-
VOUT+
VOUT-
103b

FIG. 2

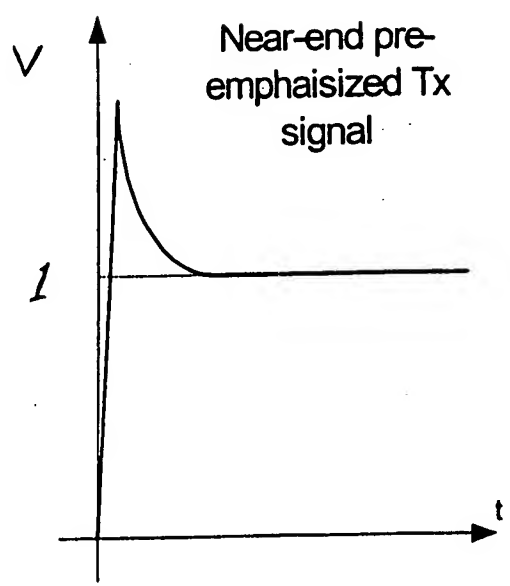

FIG. 3

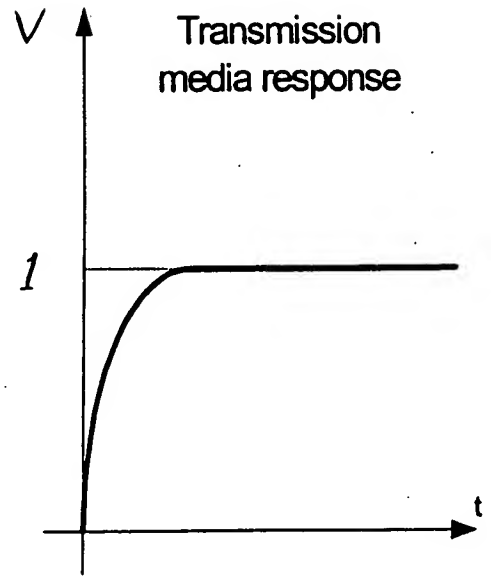

FIG. 4

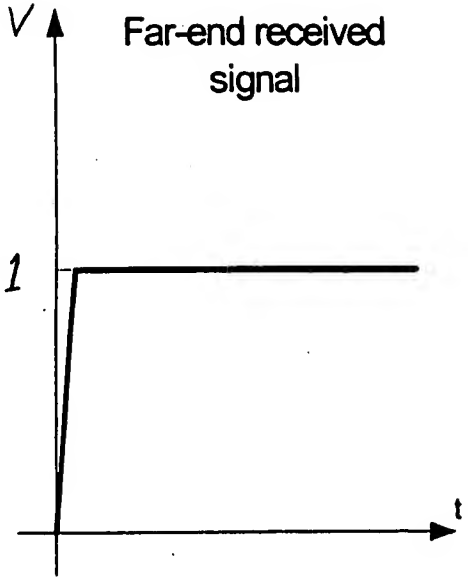

FIG. 5

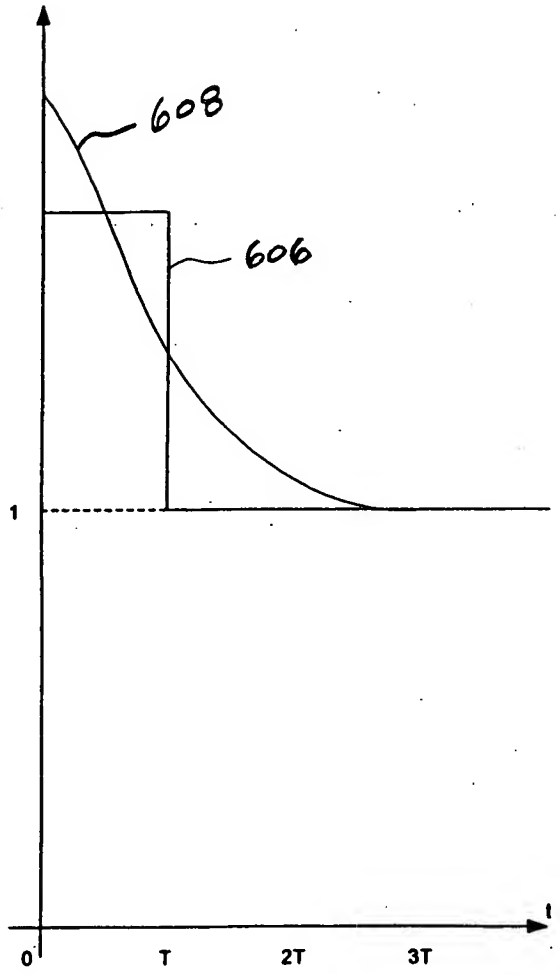
608
606
1
0
T
2T
3T
t

FIG. 6

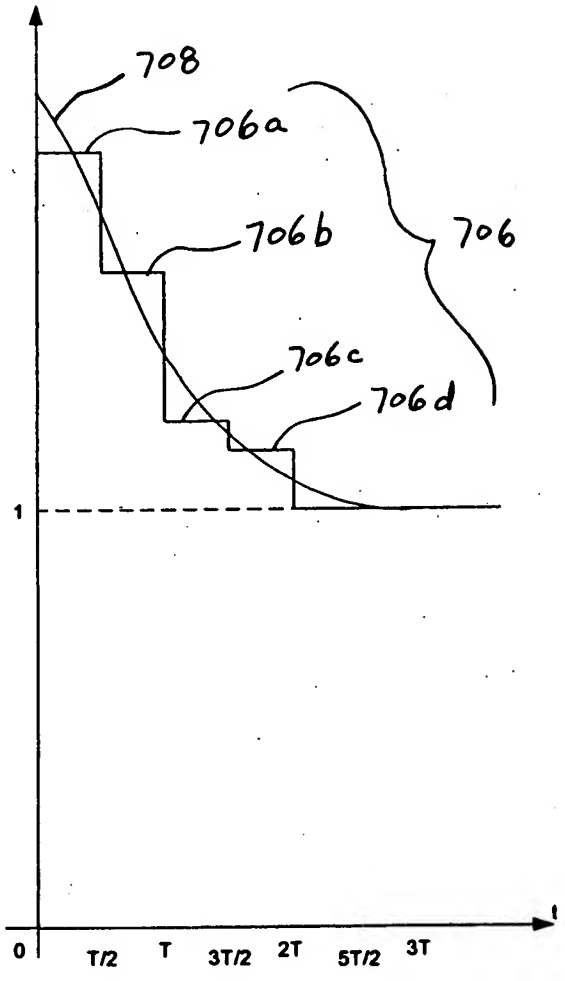
708
706a
706b
706
706c
706d
1
0
T/2
T
3T/2
2T
5T/2
3T
t

FIG. 7

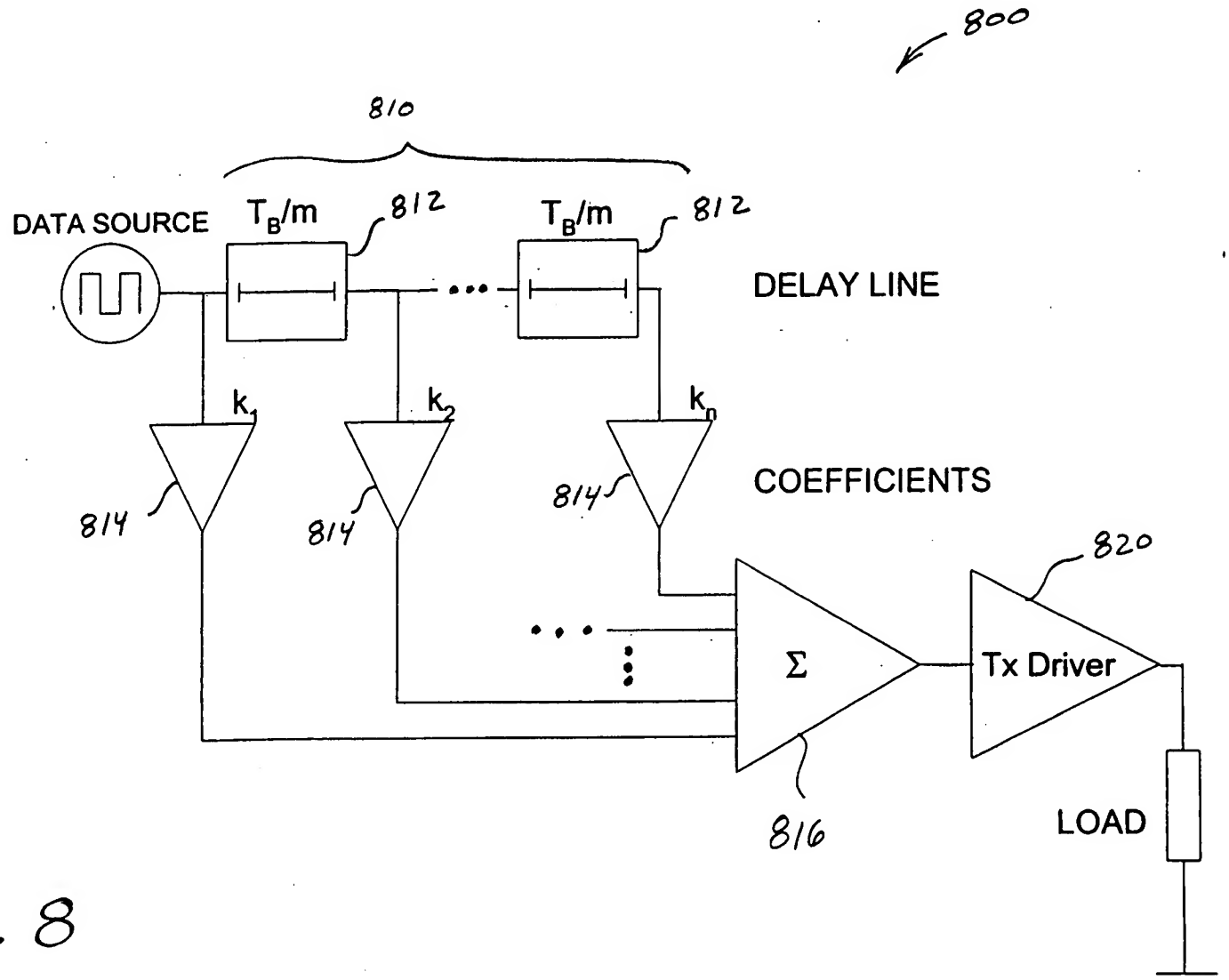
800
810
DATA SOURCE
T_B/m
812
T_B/m
812
DELAY LINE
k_1
k_2
k_n
814
814
814
COEFFICIENTS
820
Σ
Tx Driver
816
LOAD

FIG. 8

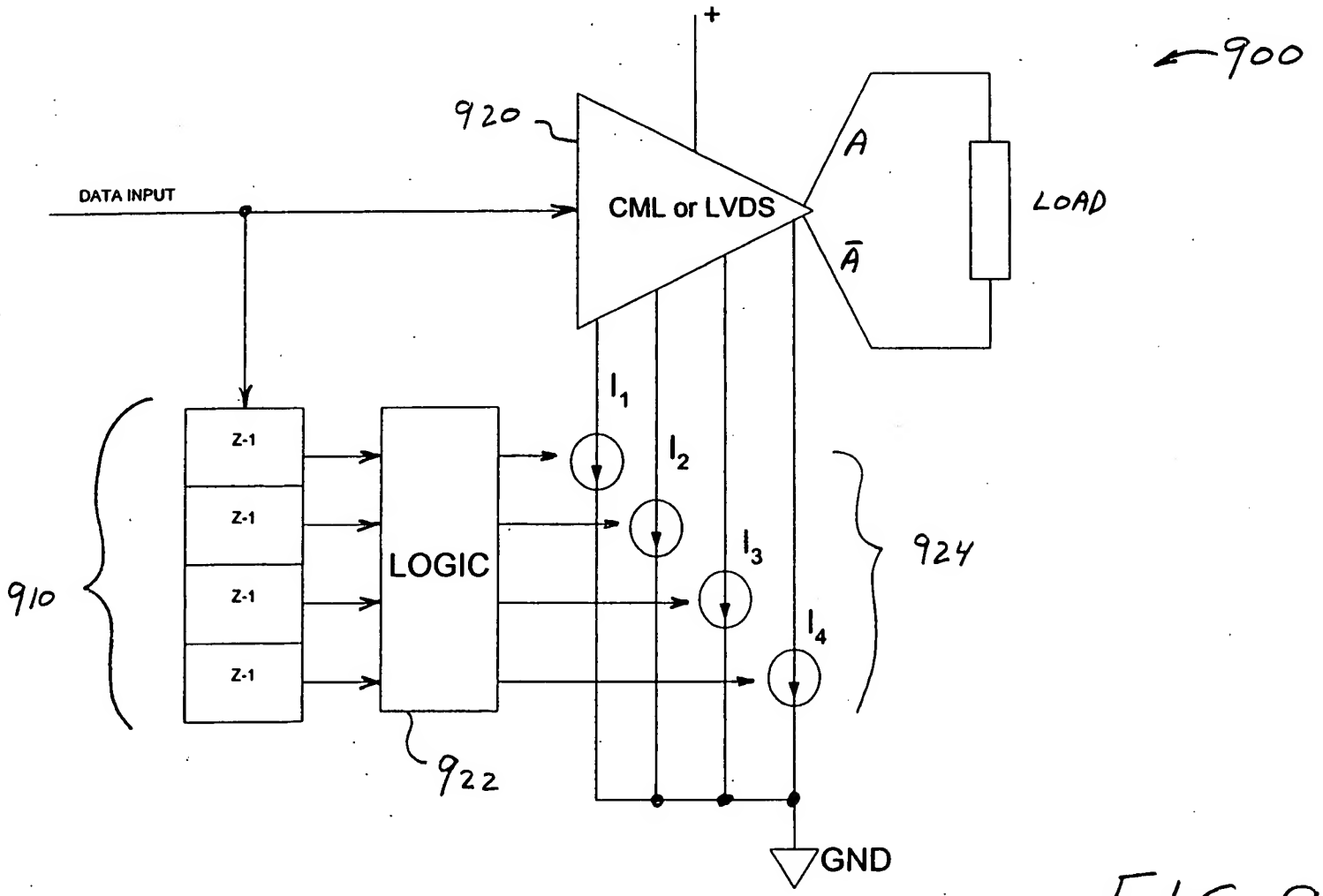
900
920
+
DATA INPUT
CML or LVDS
A
$\bar{A}$
LOAD
I_1
I_2
I_3
I_4
Z-1
Z-1
Z-1
Z-1
LOGIC
910
922
924
GND

FIG. 9

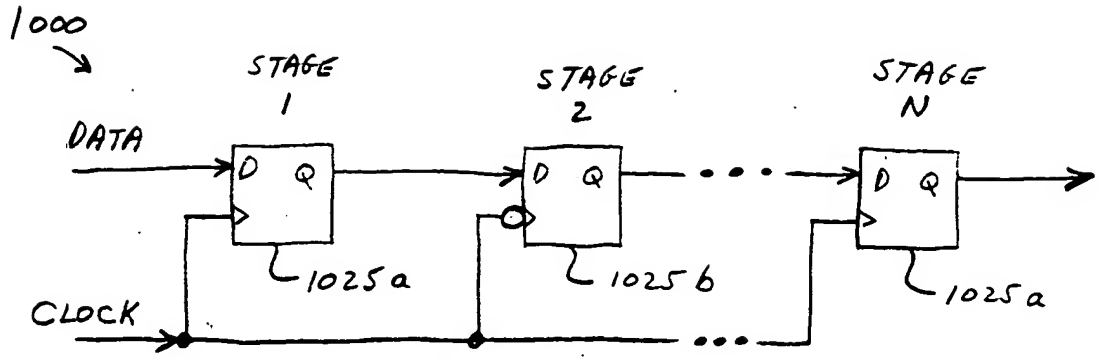
1000
STAGE 1
STAGE 2
STAGE N
DATA
D Q
D Q
D Q
1025a
1025b
1025a
CLOCK

FIG. 10

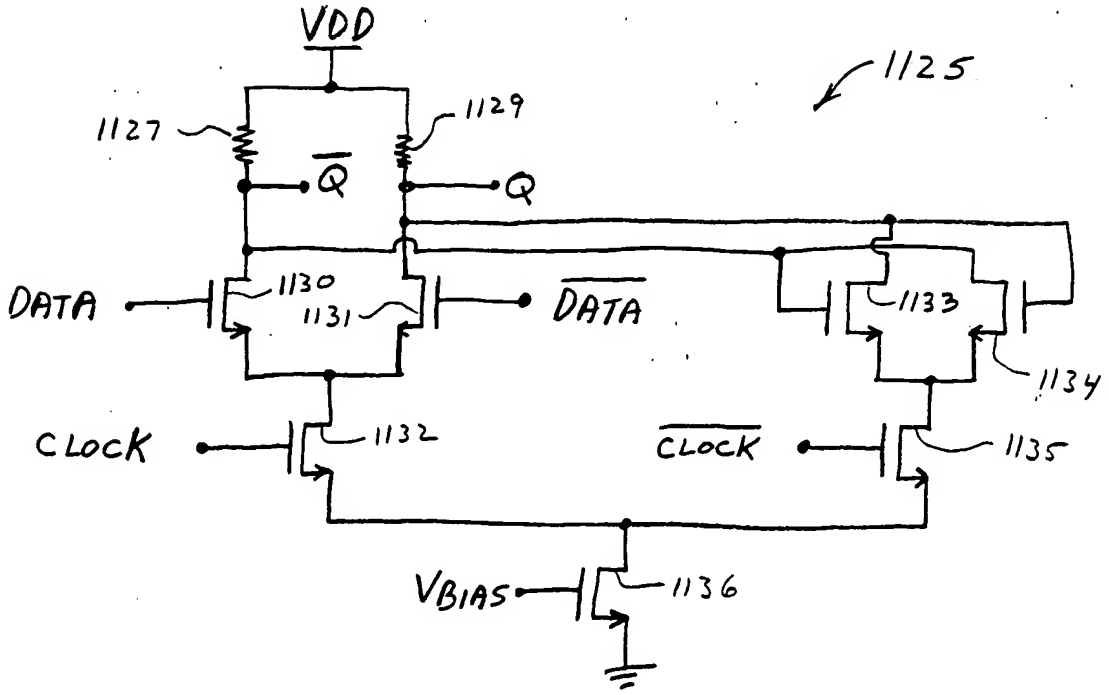
VDD
1125
1127
1129
Q
Q
DATA
1130
1131
DATA
1133
1134
CLOCK
1132
CLOCK
1135
VBIAS
1136

FIG. 11

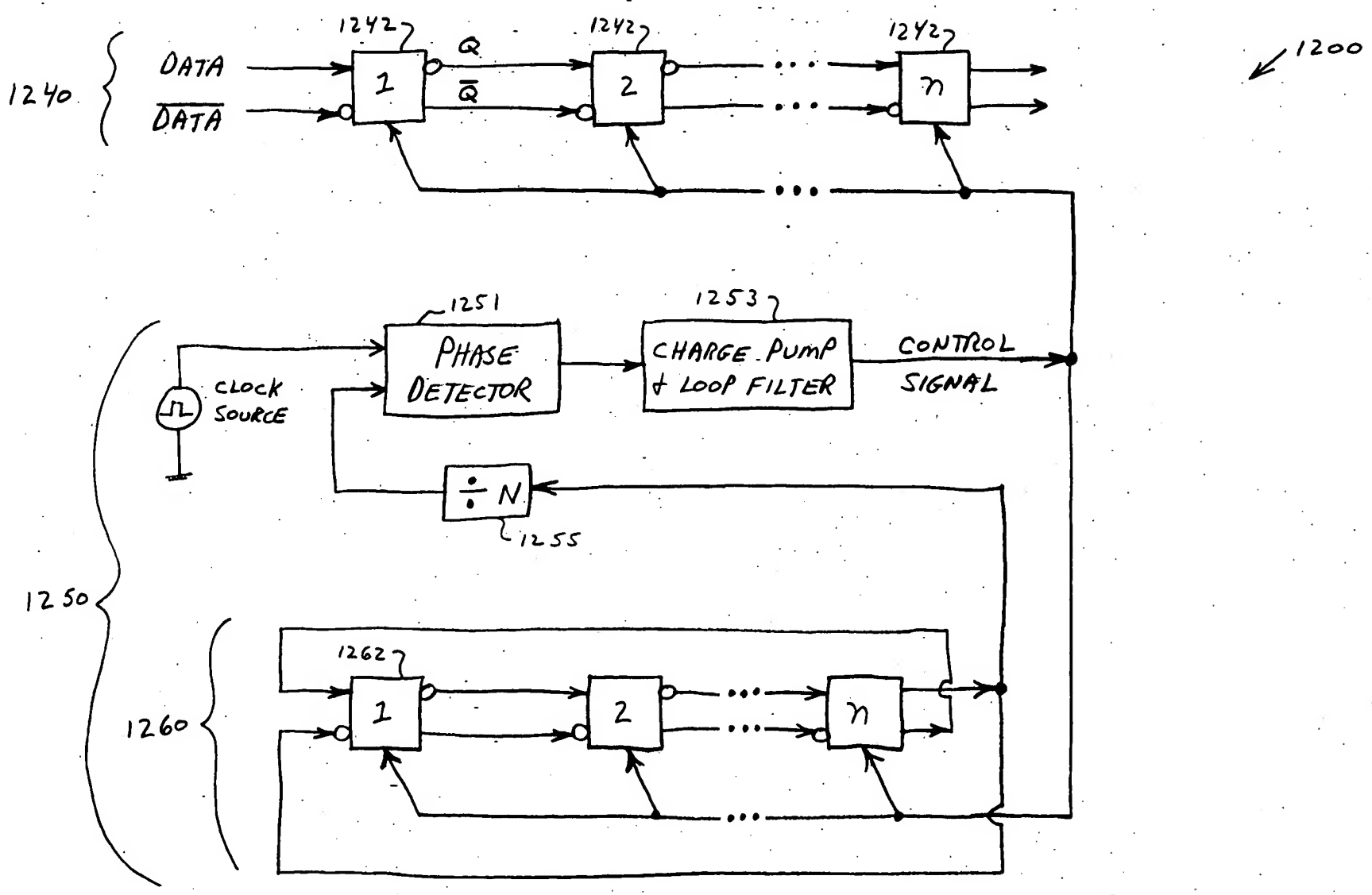
1200
1240
DATA
DATA
1242
1
Q
Q
2
n
1250
1251
PHASE DETECTOR
1253
CHARGE PUMP & LOOP FILTER
CONTROL SIGNAL
CLOCK SOURCE
÷ N
1255
1260
1262

FIG. 12

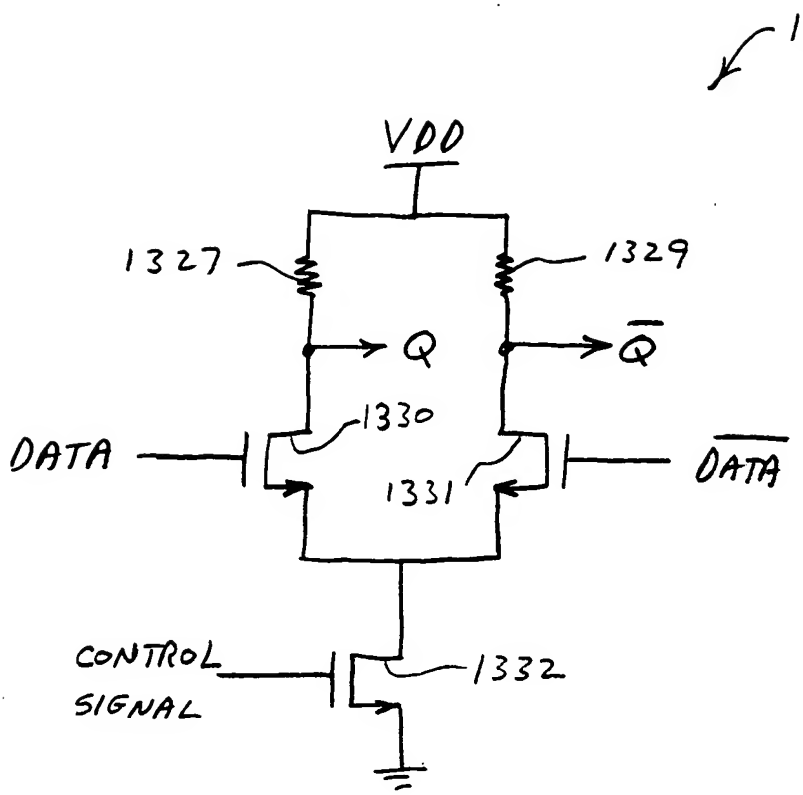
1342/62
VDD
1327
1329
Q
$\overline{Q}$
1330
DATA
1331
$\overline{DATA}$
CONTROL
SIGNAL
1332

FIG. 13

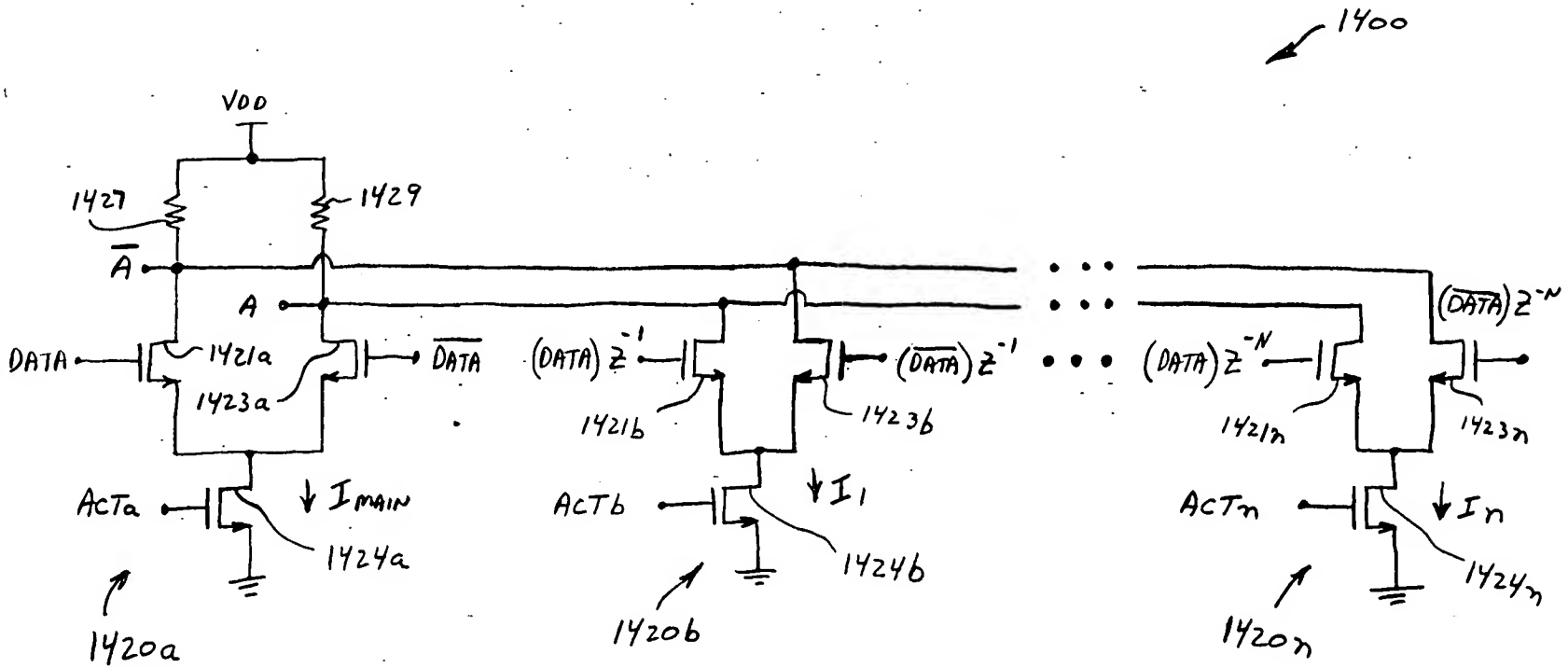
1400
VDD
1427
1429
$\overline{A}$
A
DATA
1421a
1423a
$\overline{DATA}$
ACTa
I_{MAIN}
1424a
1420a
$(DATA)z^{-1}$
1421b
1423b
$(\overline{DATA})z^{-1}$
ACTb
I_1
1424b
1420b
$(DATA)z^{-N}$
1421n
1423n
$(\overline{DATA})z^{-N}$
ACTn
I_n
1424n
1420n

FIG. 14

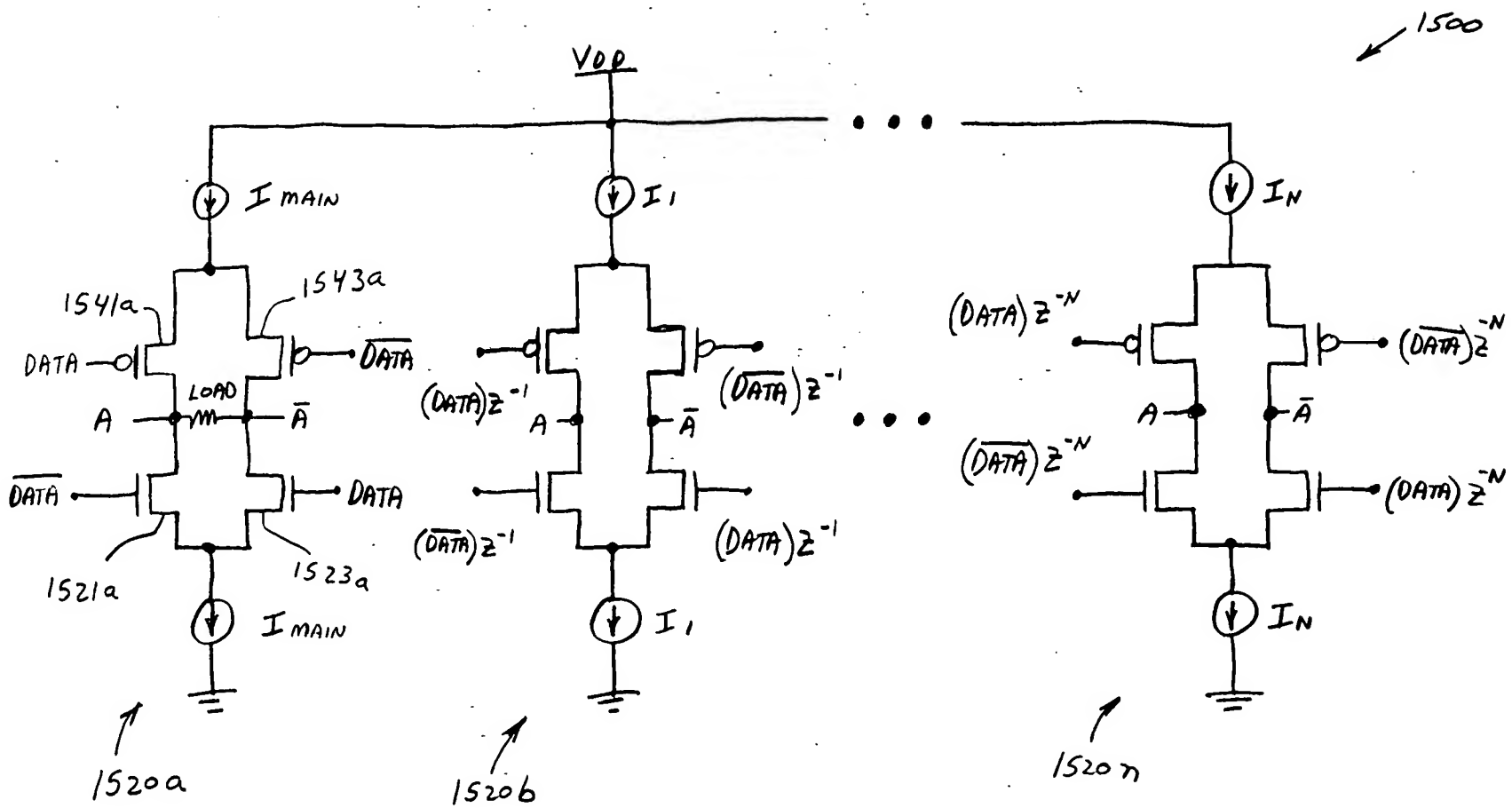
1500
VDD
I MAIN
I1
IN
1541a
1543a
DATA
DATA
LOAD
A
Ā
DATA
DATA
1521a
1523a
I MAIN
(DATA)z-1
(DATA)z-1
(DATA)z-1
(DATA)z-1
I1
(DATA)z-N
(DATA)z-N
(DATA)z-N
(DATA)z-N
IN
1520a
1520b
1520n

FIG. 15

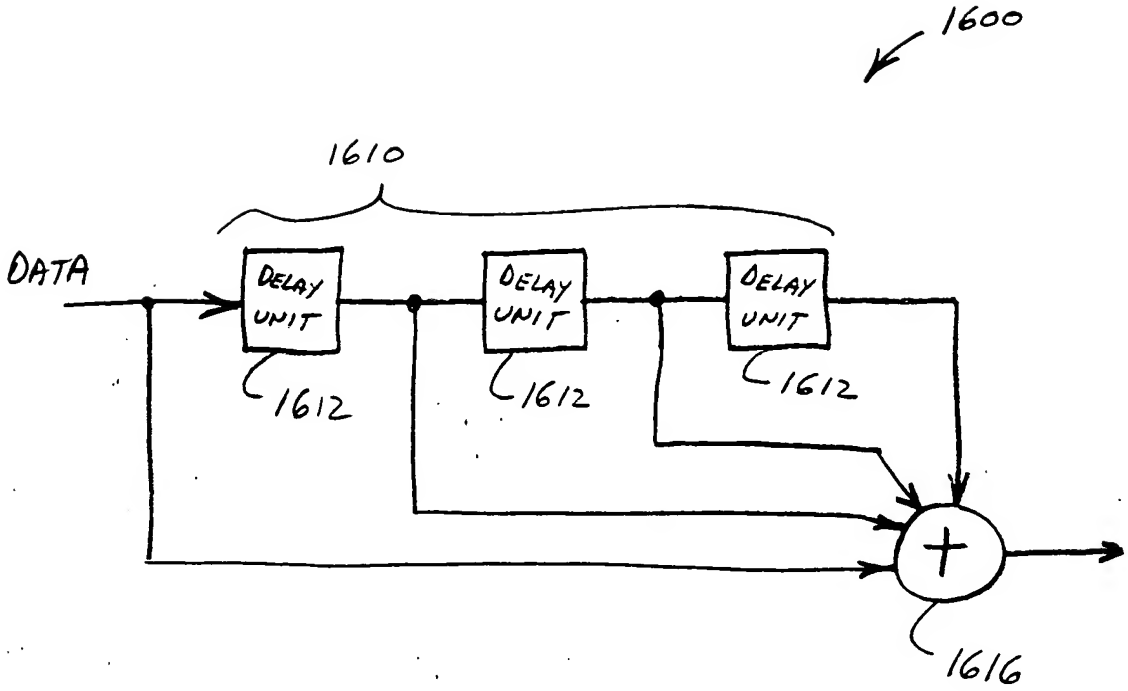
1600
1610
DATA
DELAY UNIT
DELAY UNIT
DELAY UNIT
1612
1612
1612
+
1616

FIG. 16

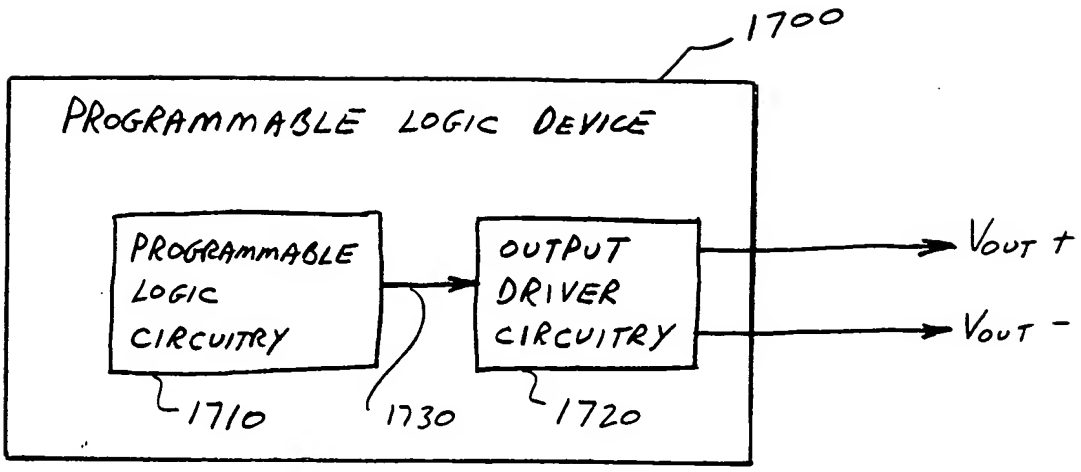
1700
PROGRAMMABLE LOGIC DEVICE
PROGRAMMABLE LOGIC CIRCUITRY
OUTPUT DRIVER CIRCUITRY
VOUT +
VOUT -
1710
1730
1720

FIG. 17

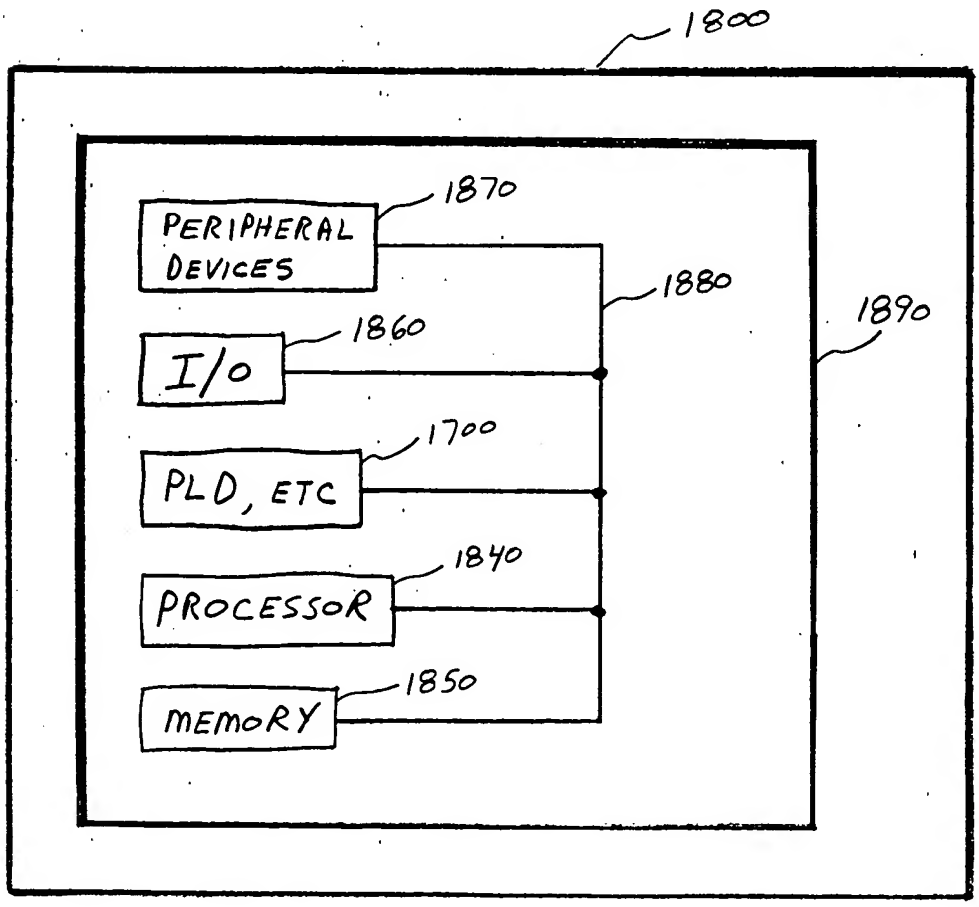
1800
1870
PERIPHERAL DEVICES
1880
1890
1860
I/O
1700
PLD, ETC
1840
PROCESSOR
1850
MEMORY

FIG. 18